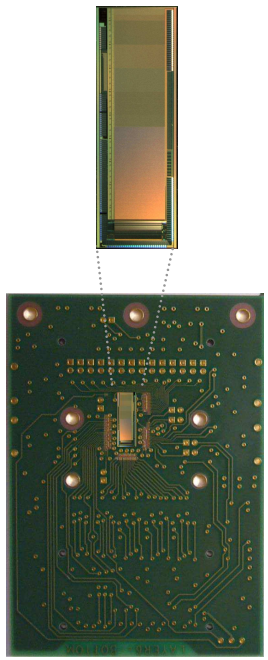
STAR Meeting, Strasbourg 3- 4 April 2008
Mimosa 22 Steering & Readout

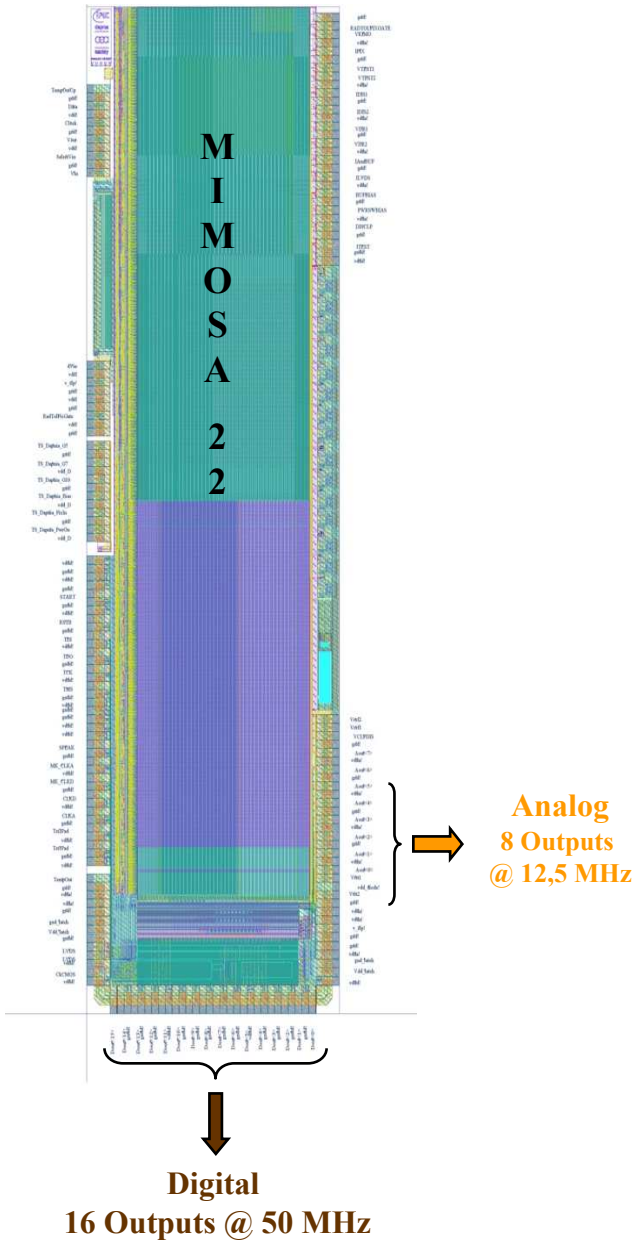


Mimosa 22
Proximity Board

OUTLINE

- **Mimosa 22 overview (DAQ point of view)**
- **Configuration by JTAG slow control**
- **Steering & Readout protocol**
- **Mimosa 22 hardware (Proximity and auxiliary boards)**
- **Testability features**
- **DAQ System example**
- **Conclusion**

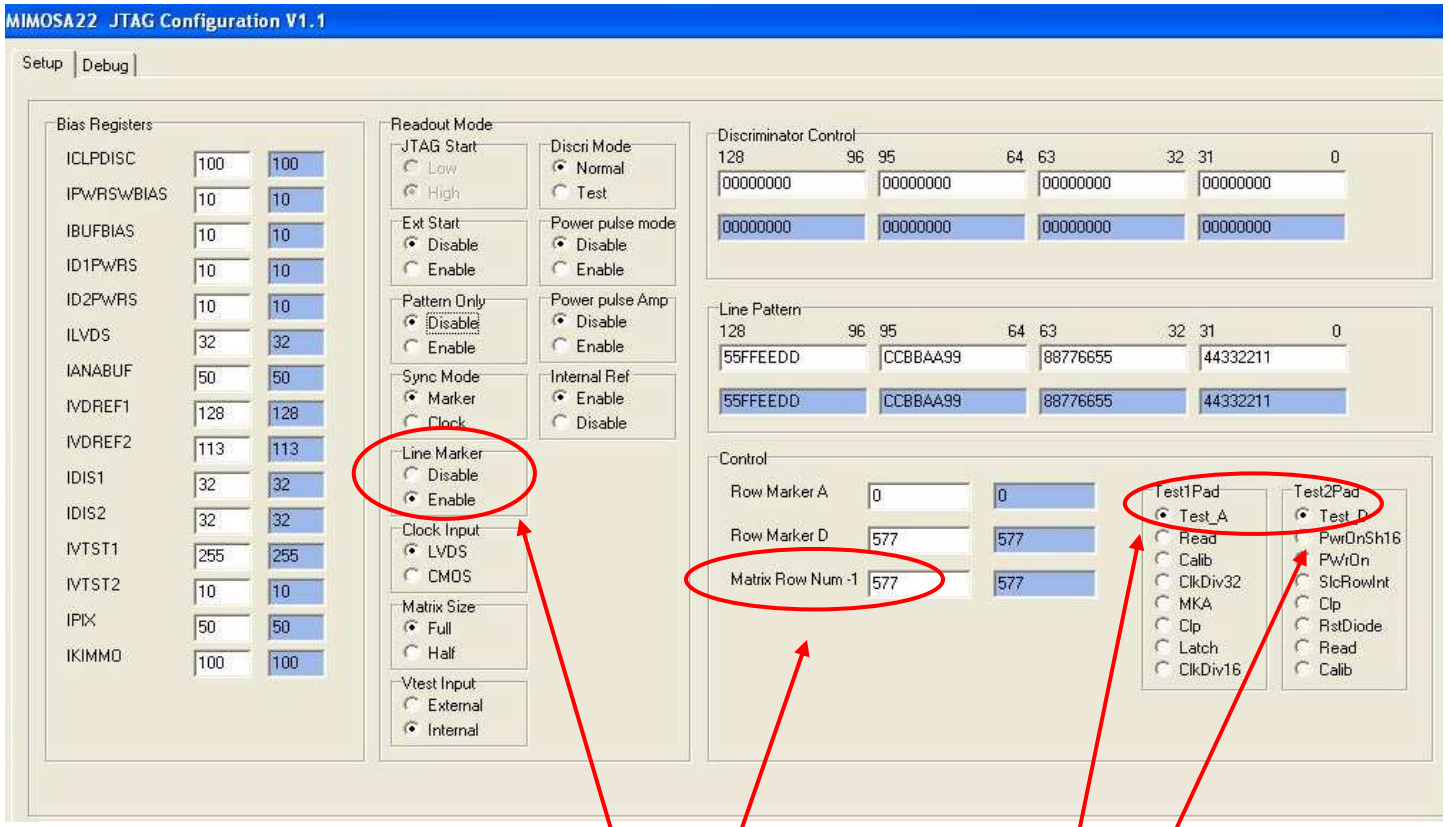
Mimosa 22 overview (DAQ point of view)



Mimosa 22 (Main clock 100 MHz – TInteg = 92,16 us)

- Analog pixels
  - 8 columns x 576 lines = 4608 pixels (17 sub-matrices)
  - Columns parallel readout on 8 Outputs
  - 2 Samples (Read & Calib) / pixel => 12,5 MHz data stream
- Digital pixels (pixel + discriminator)
  - 128 columns x 576 lines = 73728 pixels (17 sub-matrices)
  - Columns serial readout on 16 Outputs (8 columns / output)
  - 1 bit / pixel => 50 MHz data stream
- Main testability features
  - 2 Markers lines can be added at the end of matrix (Total = 578 lines)
    - Analog signals emulated by two fixed level
    - Discriminators state replaced by a fixed pattern
  - Internal pulse generator to test / characterize discriminators
- Configuration
  - All parameters (operating modes, bias) configurable by JTAG

Configuration by JTAG slow control



JTAG software

- Running under Windows
- PC // port HW interface
- Data rate ~ 100 kbit/s

Development done by K.Jaaskelainen

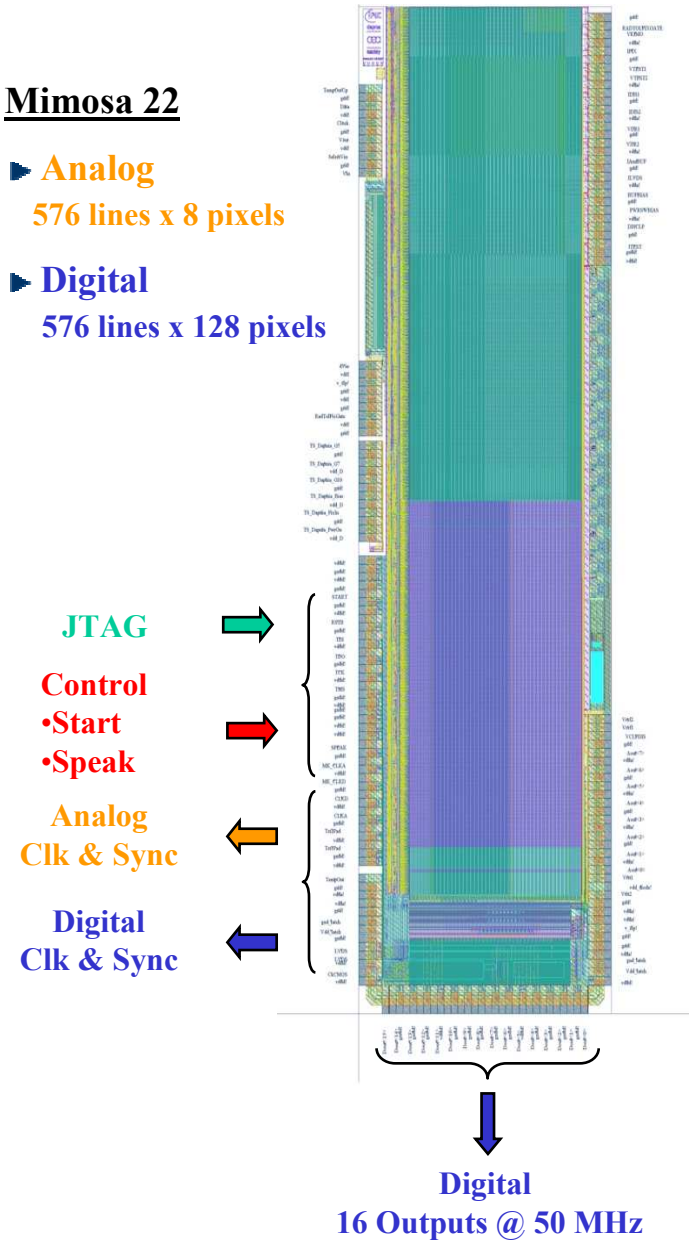
Mimosa 22 … Many operating modes …

- **Default configuration suggested :**
  - Add the two markers lines at end of matrix
  - Select analog and digital markers as test signals
    - Test1Pad = Test_A = MK_TEST_A (Analog marker)
    - Test2Pad = Test_D = MK_TEST_D (Digital marker)

Steering & Readout protocol : Signals overview

Mimosa 22

- Analog
  576 lines x 8 pixels
- Digital
  576 lines x 128 pixels



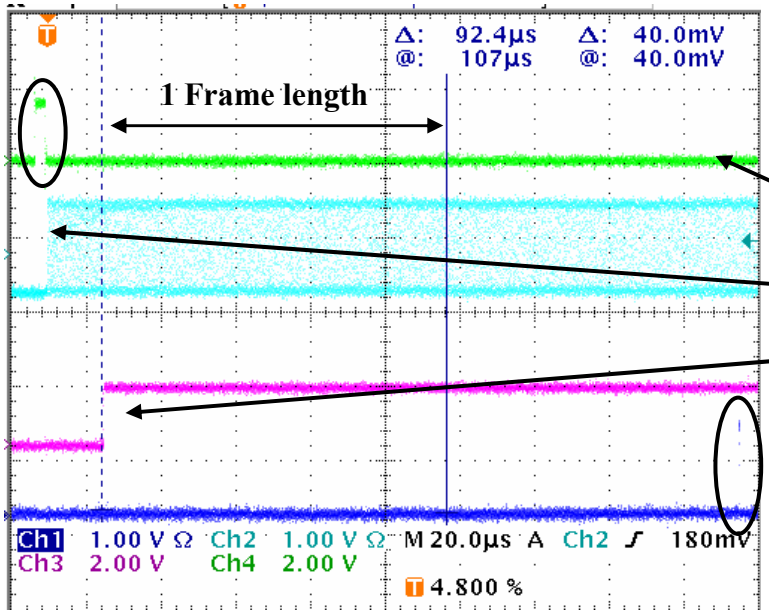
Mimosa 22 Control

- Operating modes and bias configuration by JTAG
- Two steering lines
  - Start
    To synchronize all Mimosa 22 (Hopefully). No clock signal before Start.
  - Speak
    Mi22 provides data when Speak = 1. No synchronization signal if Speak = 0.
    Acts as a DAQ_READY signal (set to 0 while DAQ is BUSY).

Mimosa 22 DAQ Synchronization

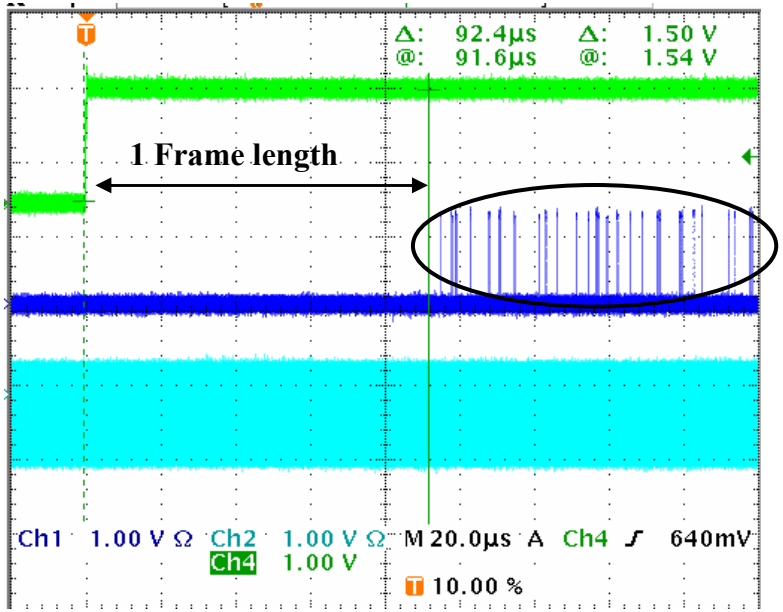
- Separate clock & sync signals for analog & digital outputs
  - Analog
    - CLK_A — Clock for analog data
    - MK_CLK_A — Synchronization on last line
  - Digital
    - CLK_D — Clock for digital data
    - MK_CLK_D — Synchronization on last line, last pixel
- Test markers – Line configurable by JTAG
  - MK_TEST_A (Analog) / MK_TEST_D (Digital)

Steering and Readout protocol : Start and Speak phases



Start and Speak Phases

- Start signal used to synchronize all Mimosa 22 (We hope …)
- Start signal => Starts all clock generation
- Clock (Analog & Digital) starts after Speak pulse
- Speak signal (after Start pulse) => Starts all Sync generation
- Sync (Analog & Digital) occurs at least one frame after Speak



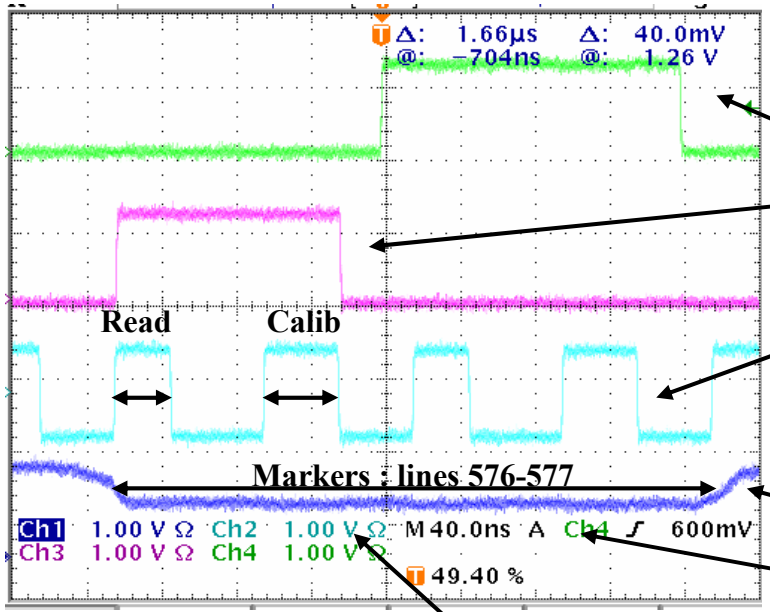
Speak Phase

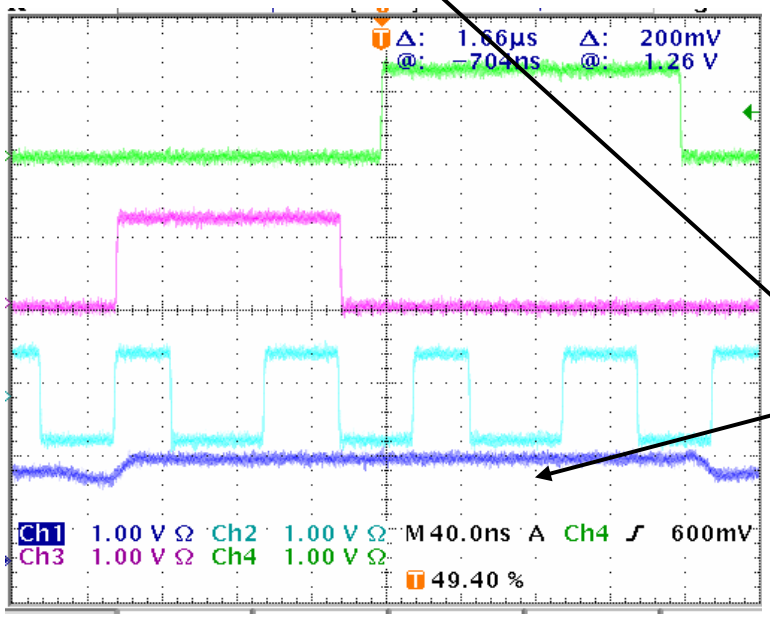
- Accumulation of N Sync signals after Speak rising edge
- No Sync signal during the frame where Speak occurs

Why Speak signal ?

- DAQ development easier (Multiple boards synchronization)
  - Our DAQ can't store consecutives events without dead time
- Can be let at 1 if / while DAQ has no dead time (double buffer)

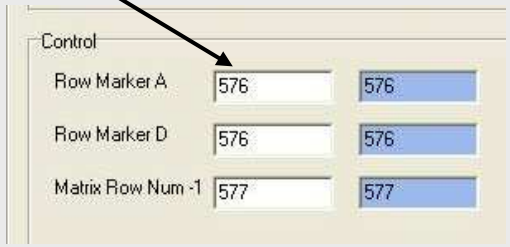
Steering and Readout protocol : Analog synchronization

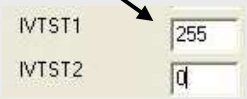




Analog synchronization (578 lines)

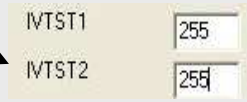
- SYNC_A signal : occurs on last line : 577 – One line length
- MK_TEST_A occurs on line 576 (Configured by JTAG)
- Analog clock : Read and Calib phases
- Analog signal
  - Pixels level on line 0-575
  - On markers lines (576-577) : Read = IVTest2 + IVTest1 - Calib = IVTest2



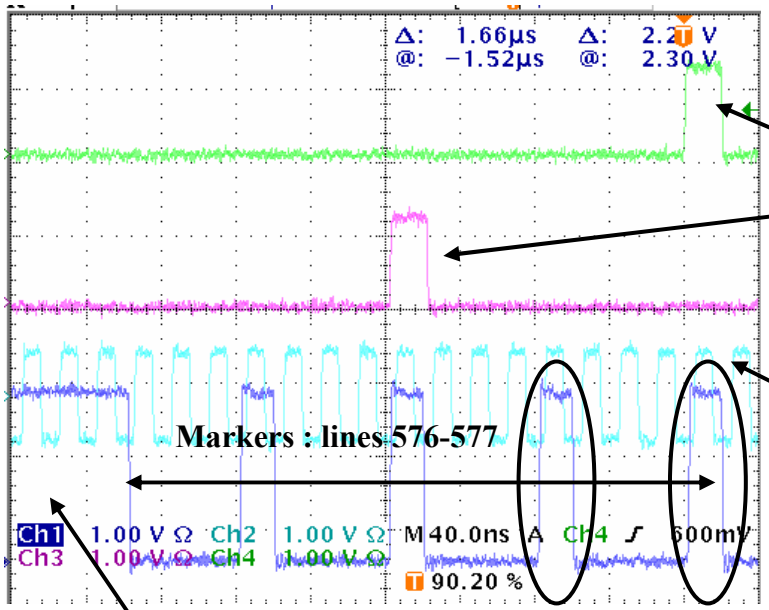


Markers lines finding by moving IVTest2

- On top scop plot IVTest2 = 0 udac
- Now IVTest2 = 255 udac => Analog level changes on lines 576-577

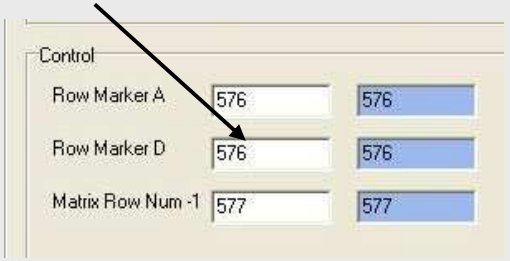


Steering and Readout protocol : Digital synchronization



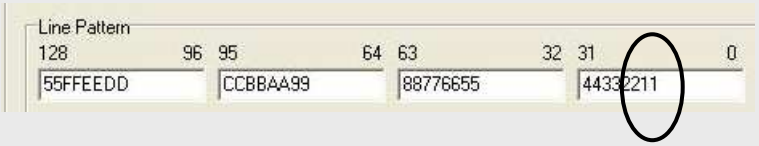
Digital synchronization (578 lines)

- SYNC_D signal : occurs on last pixel of last line : 577 – One PIXEL
- MK_TEST_D occurs on last pixel of line 576 (Configured by JTAG)
- Digital clock
  - (Main clock / 2 = 50 MHz)

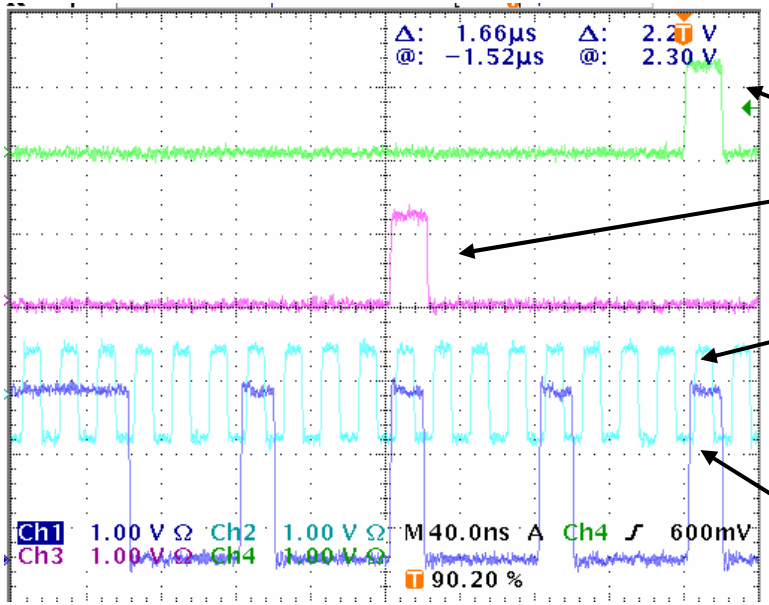


- Digital data : Output 0 = columns 0 .. 7
  - Pixels discriminator state on line 0-575
  - On markers lines (576-577) : Pattern defined by JTAG
  - 8 columns serialized on 1 digital output

Markers lines pattern
Col 0 = 1 – Col 1..3 = 0 – Col 4 = 1 – Col 5 .. 7 = 0

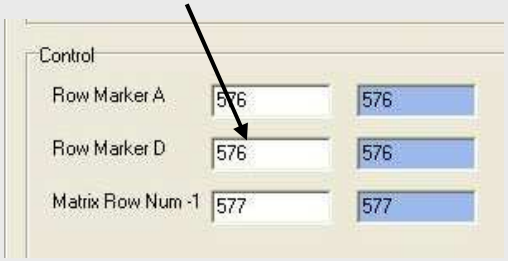


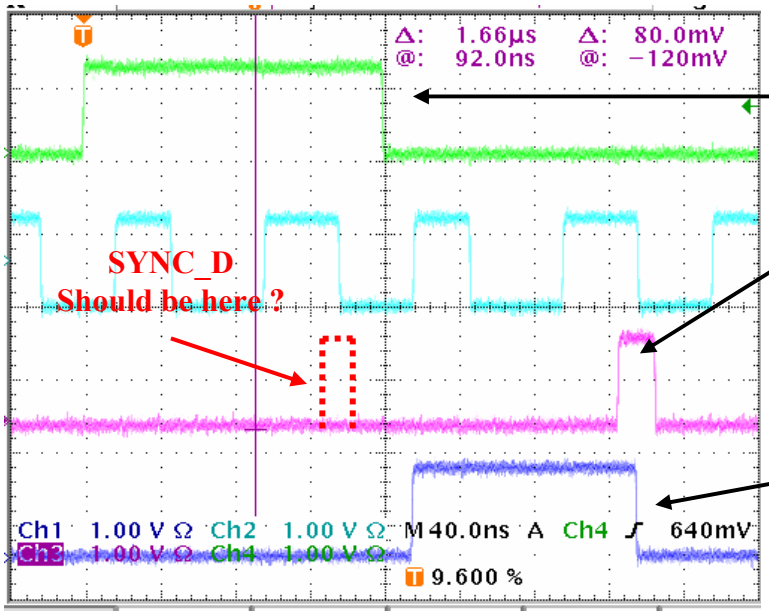
Steering and Readout protocol : Summary



Digital synchronization (578 lines)

- SYNC_D signal : occurs on last pixel of last line : 577
- MK_TEST_D occurs on line 576 (Configured by JTAG)
- Digital clock
- Digital signal (SYNC_D occurs during LSB)

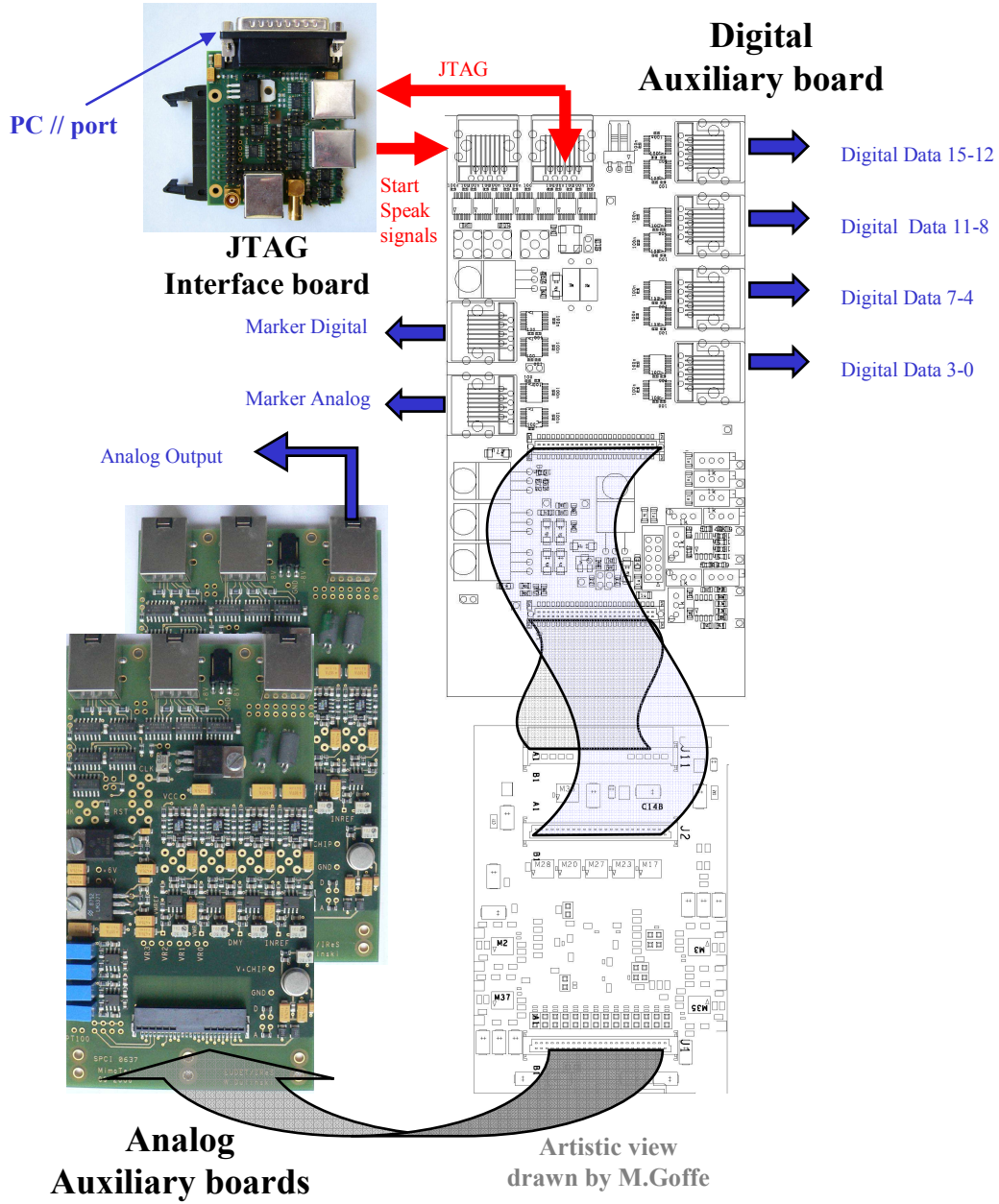




Digital / Analog synchronization …

- SYNC_A signal : occurs on last line : 577 – One line length
- SYNC_D signal : occurs on last line : 577 – One pixel length
  - BUT … SYNC_D seems to occur one line too late / SYNC_A !
- Digital data occurs one line after analog data
  - Discriminator “processing” (Need analog read & calib signal)
  - 8 columns serialization on one output
- MK_TEST_A on line 0
- Shows that digital link provides data of line 577 while analog link provides line 0

Mimosa 22 Hardware : Proximity & auxiliary boards



Four boards

- Proximity board
  - Mimosa 22 is bonded on it
  - First level of buffers & amplifiers
- Digital auxiliary board
  - Proximity board power supply
  - Clock generator
  - Digital signals buffers
- JTAG interface board
  - PC // Port to LVDS translators
- Analog auxiliary boards
  - Analog signals amplifiers (SE / DIFF)
  - Two boards are required (4 channels / board)

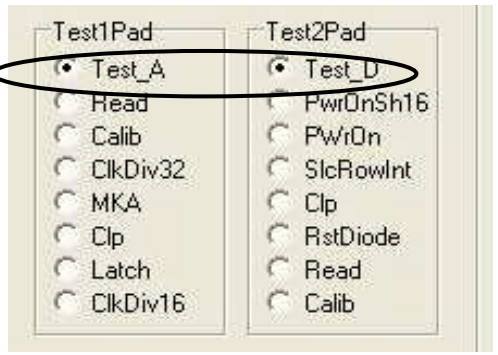
- Boards designed by W.Dulinski
- Documentation by M.Goffe & M.Specht

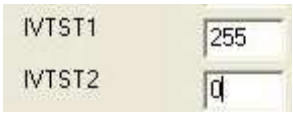
Testability features : DAQ point of view

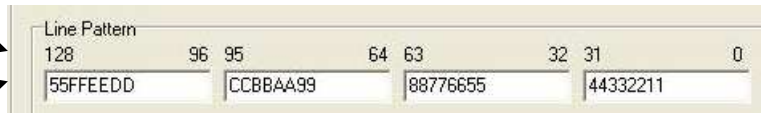
Mimosa 22 testability dedicated to DAQ

- Two configurable test signals
  - Markers on analog & digital data (Line configurable)
  - Mimosa 22 internal signals
- Two extra markers lines – in data flow - at end of matrix
  - Analog outputs : read & calib emulation by fixed level
  - Digital outputs : Fixed pattern
- Digital pattern generator
  - Replace pixels data by the marker line on ALL lines
  - Useful to check digital data link from Mimosa 22 to DAQ

JTAG software parameters



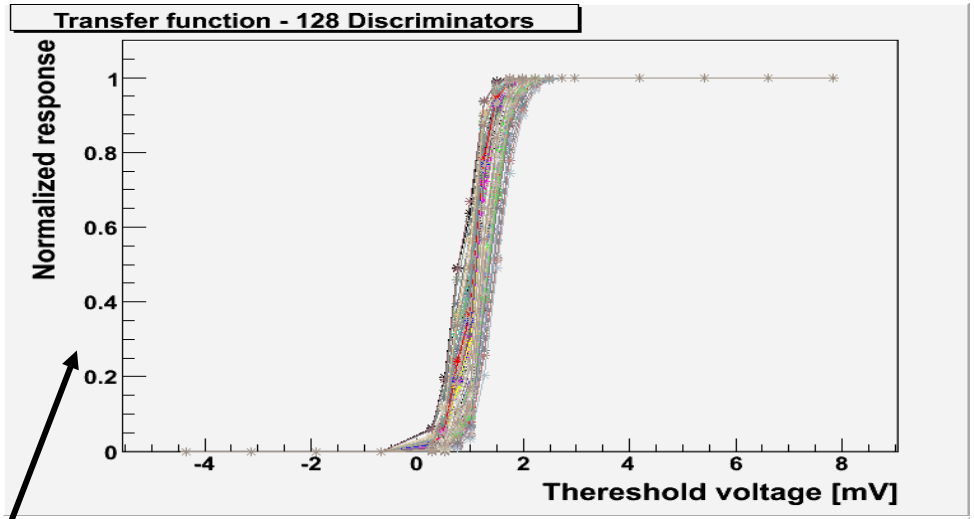


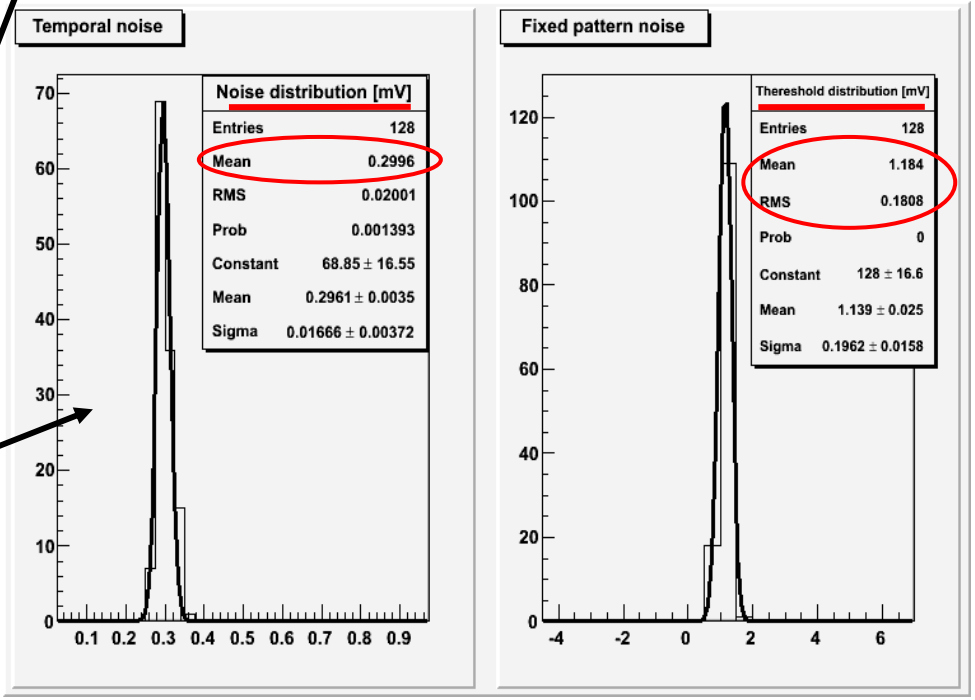


Testability features : Test point of view

Testability dedicated to characterization

- Possibility to disable noisy columns (Digital pixels)
- Internal pulse generator to test discriminators
  - Emulate pixels signals
    - Read = VTest2 + VTest1 & Calib = VTest2
      - VTest2 = base line : 0 .. 2500 mV – 10 mV step
      - VTest1 = signal : -30 .. +34 mV – 0,25 mV step
  - Discriminators threshold
    - Threshold = VRef1 – VRef2
      - VRef2 = base line : 0 .. 2500 mV – 10 mV step
      - VRef1 = signal : -30 .. +34 mV – 0,25 mV step
- Example of discriminators characterization
  - Threshold set to 1 mV
  - Input scan from -4 mV to +8 mV
  - Results
    - Threshold 1,18 mV
    - Threshold dispersion 180 uV
    - Mean noise 300 uV





Analysis software developed by M.Gélin - IRFU

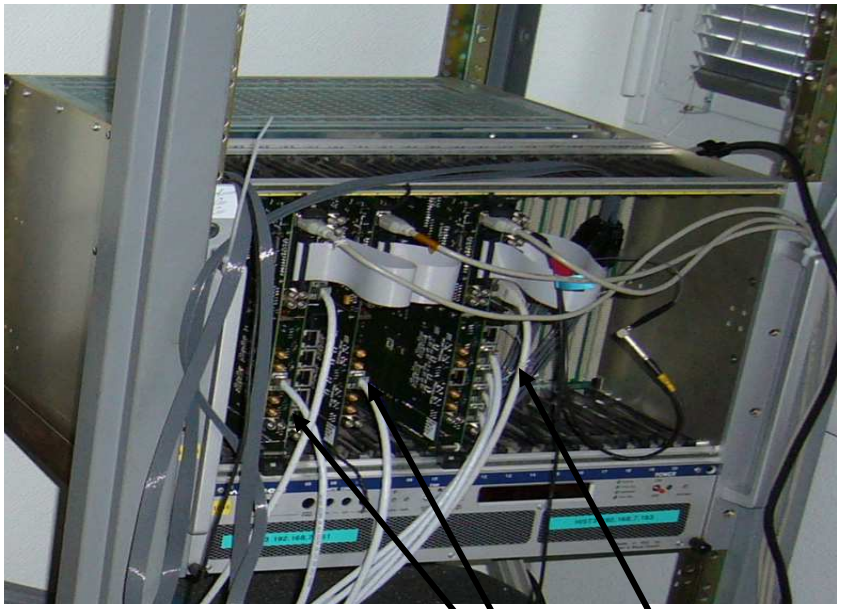
Testability features : Phase 1

Testability & Readout on Phase 1 (640 columns x 640 lines)

- **Features of Mimosa 22**
  - Markers – Discriminators test generator – Digital pattern generator
  - 8 columns / 640 can be read in analog mode (Nominal TInteg = 640 us) => Pixels characterization
  - Slow readout links : 8 analog outputs @ 2 MHz & 16 digital outputs @ 40 MHz
- **New features**
  - Readout of all columns in analog mode (80 x Nominal TInteg = 51,2 ms) => Pixels functional test
  - Frame tag (0..9) to detect desynchronization between Mimosa 22 on a ladder
  - Fast readout links : 4 digital outputs (160 MHz)

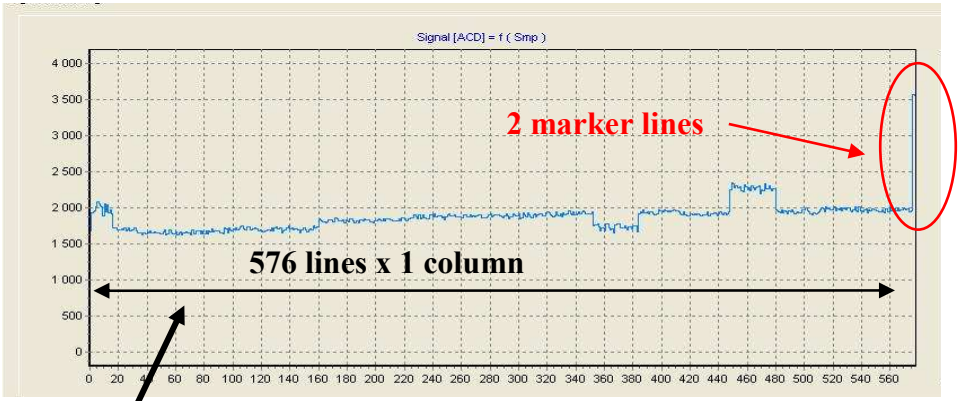
More information in Andrea's talk …

DAQ System example

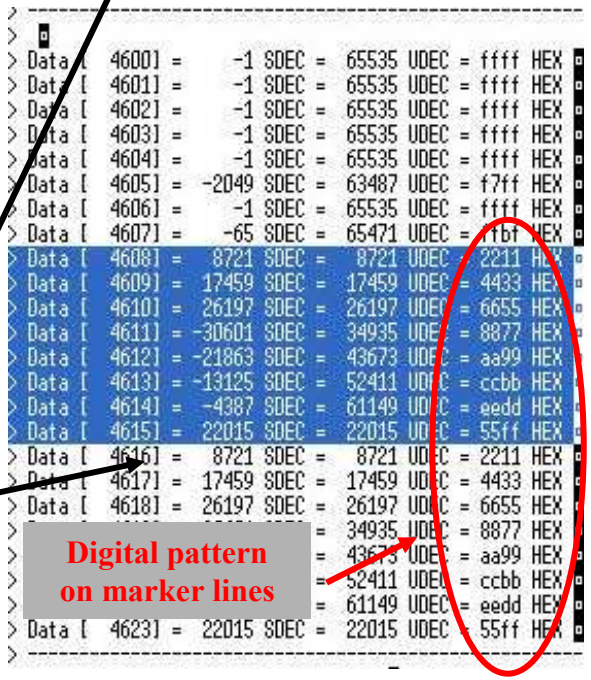


- IPHC Imager boards
  - 8 Analog outputs => 2 Boards
  - 16 Digital outputs => 1 Board + Digital extension
- On-line monitoring plots
  - Analog pixels : read signal
  - Digital pixels

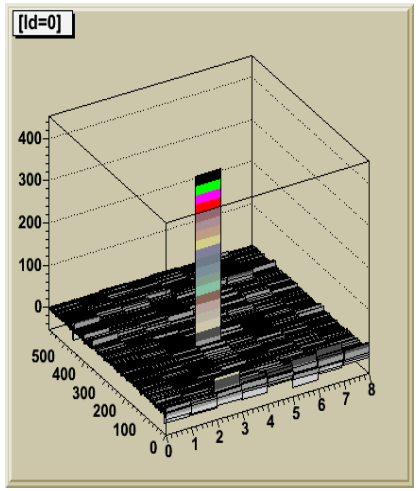
Analog pixels : Read signal



Digital pixels



Hit on Analog matrix



Conclusion : Status & Next steps

- **Mimosa 22 characterization**
  - Tests are on the way at IPHC, done by M.Goffe & Will start on next weeks at IRFU
  - First results presented by A.Dorohkov – Irradiation tests will also follow
- **Mimosa 22 hardware & software available for STAR collaboration**
  - One set of boards (Ready in next weeks) & JTAG software
  - More documentation … as soon as possible …
- **Mimosa 22 beam-tests**
  - Beginning of August at CERN
  - DAQ upgrade and integration for BT : May - July
- **Phase 1 Test & Characterization**
  - Characterization with " low speed links " : DAQ ~ Ready ⇔ Mimosa 22
    - Analog pixels on 8 links up to 50 MHz
    - Digital pixels on 16 // links up to 50 Mbit/s / link
  - Focus on Phase1 tests on PCB – Few hope do probe tests this year at IPHC
  - Fast digital link will be tested with logic analyser and Phase 1 pattern generator